FIG. 1
(PRIOR ART)

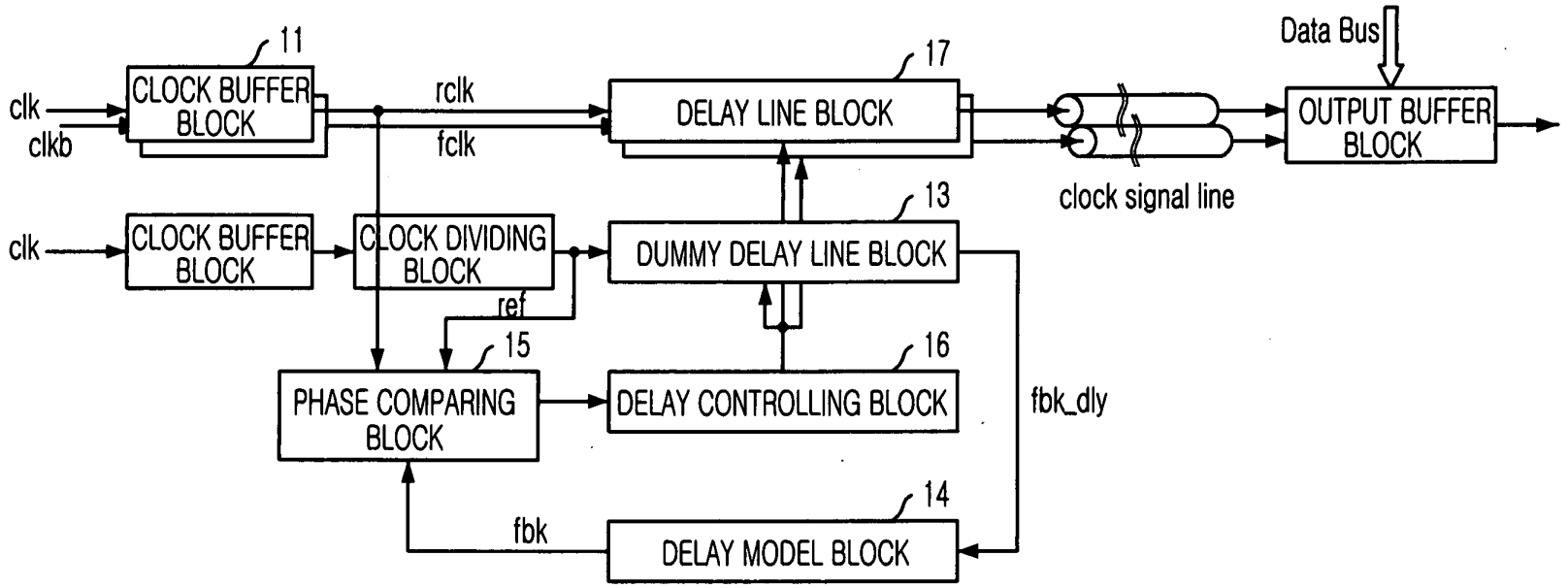


FIG. 2
(PRIOR ART)

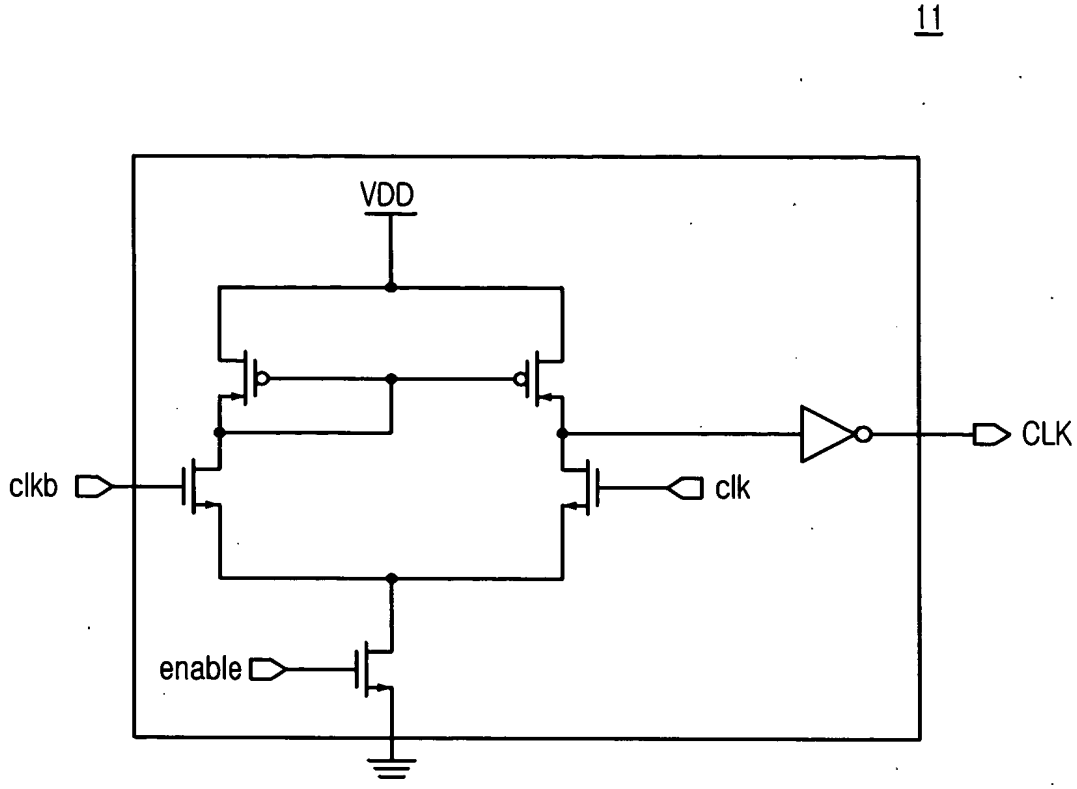
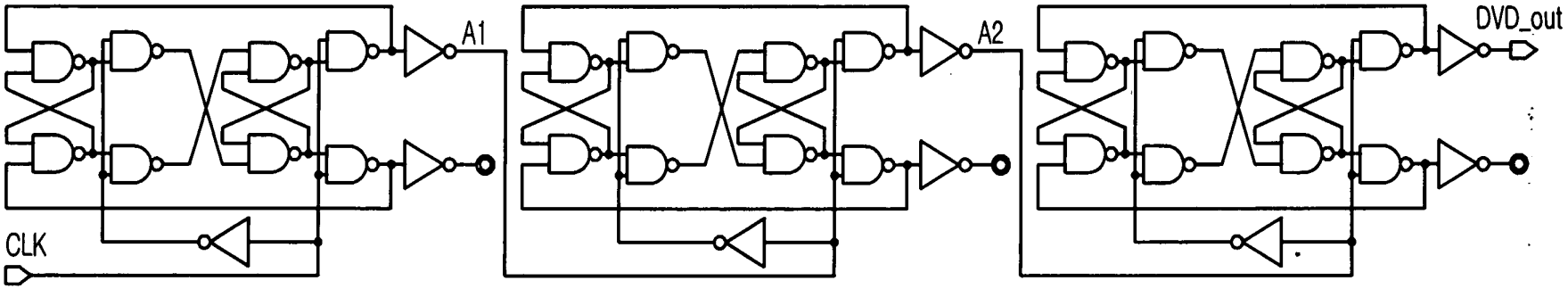


FIG. 3
(PRIOR ART)

12



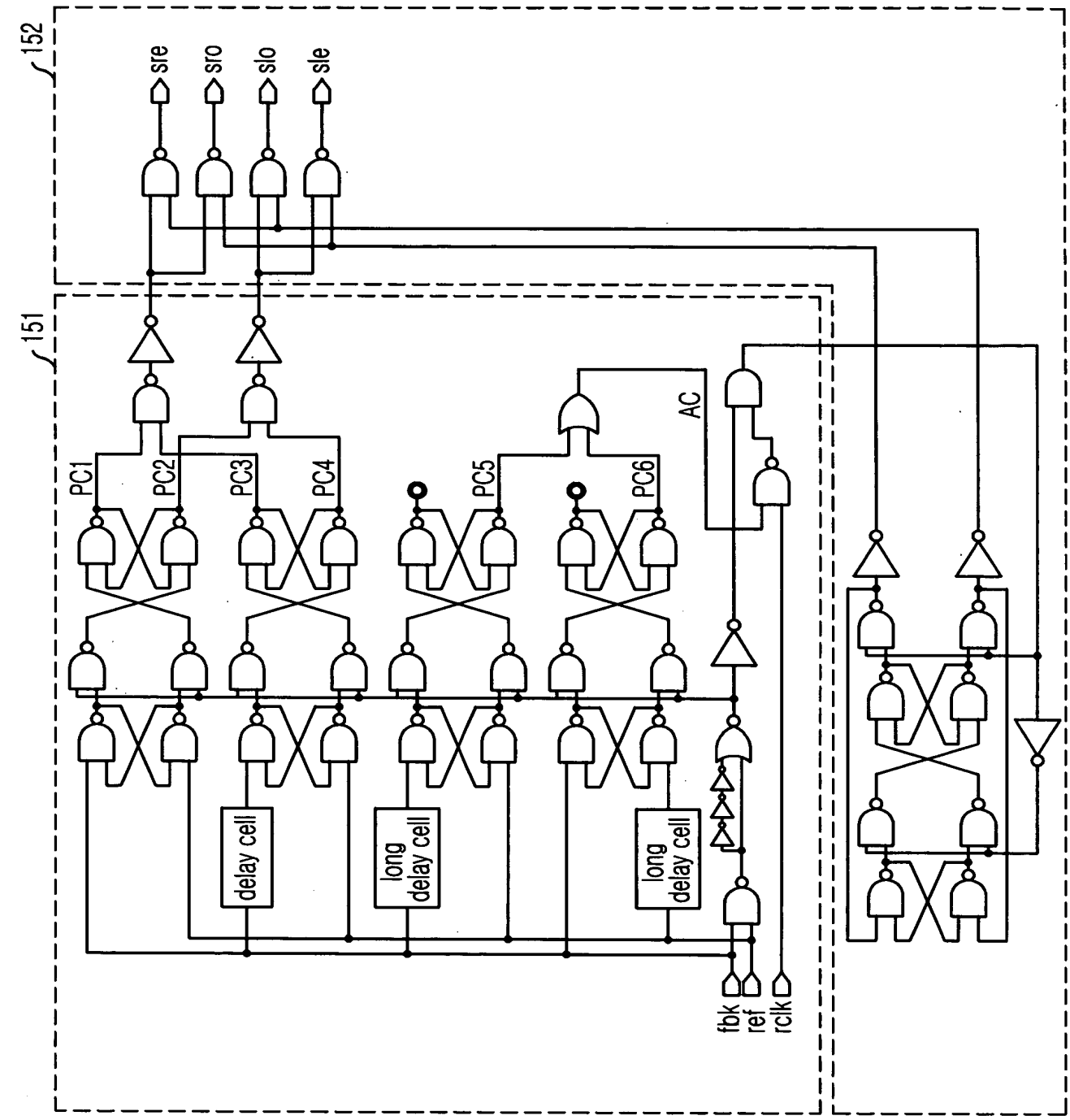


FIG. 4
(PRIOR ART)

FIG. 5
(PRIOR ART)

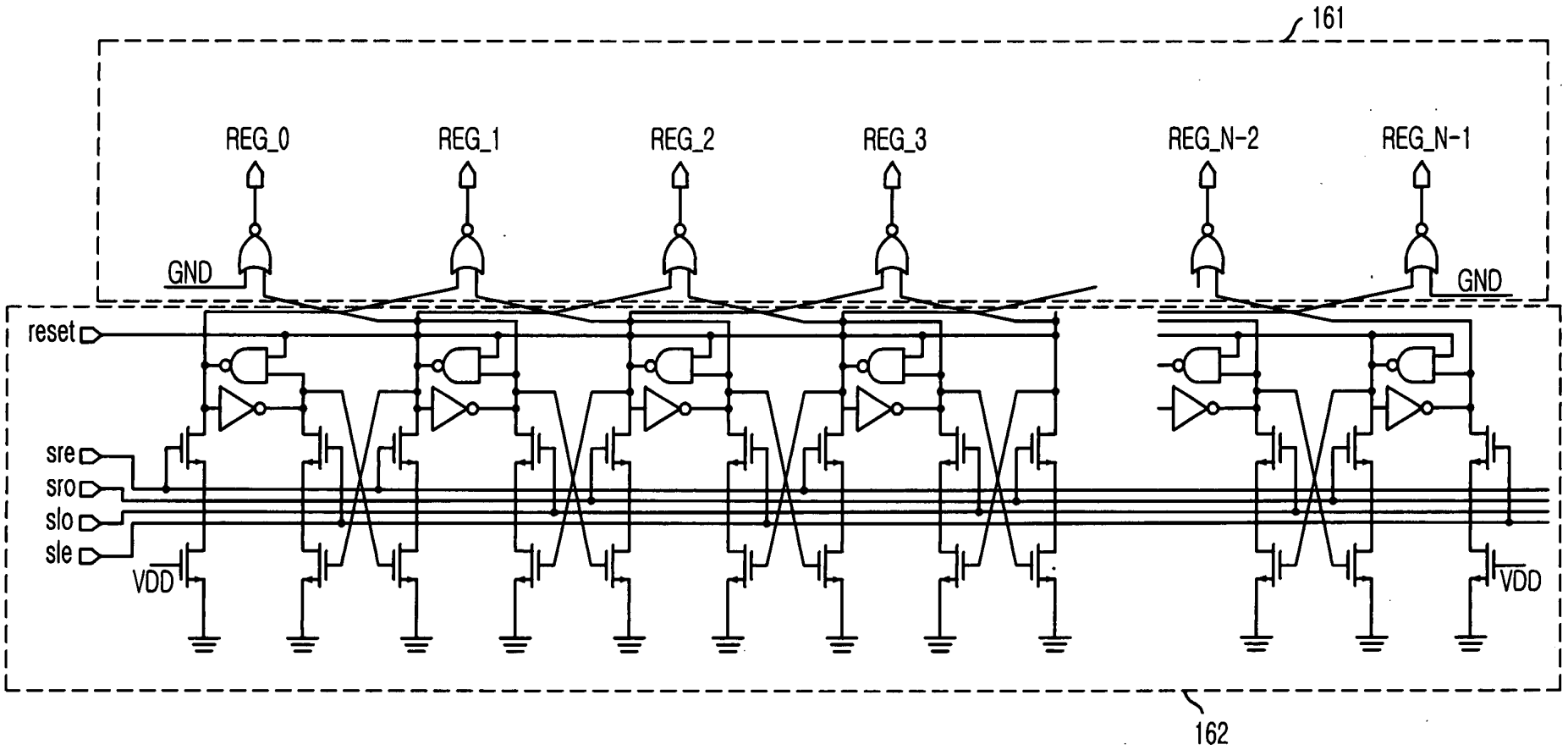


FIG. 6
(PRIOR ART)

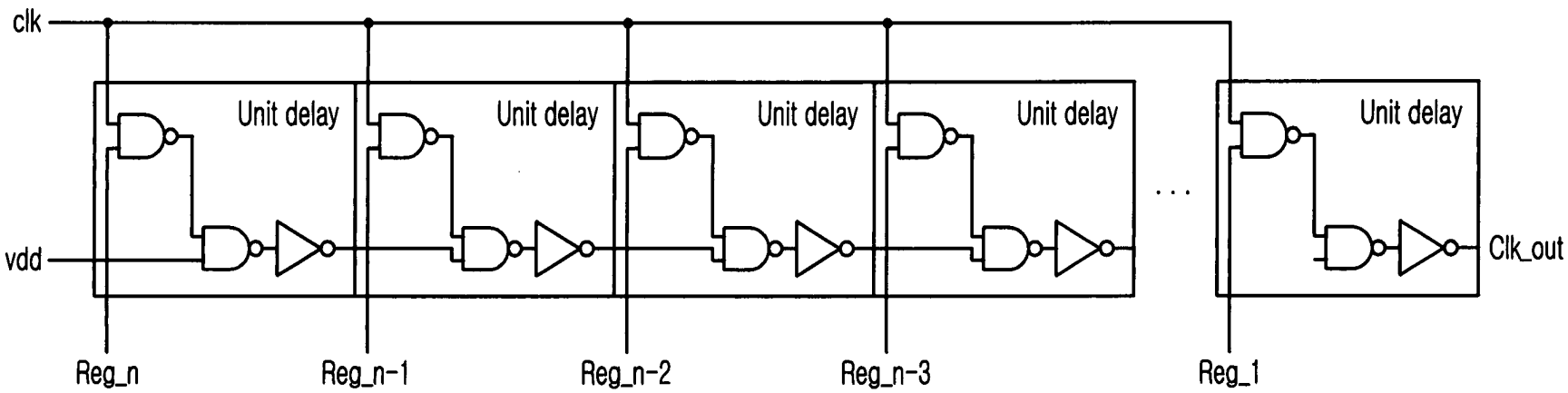


FIG. 7

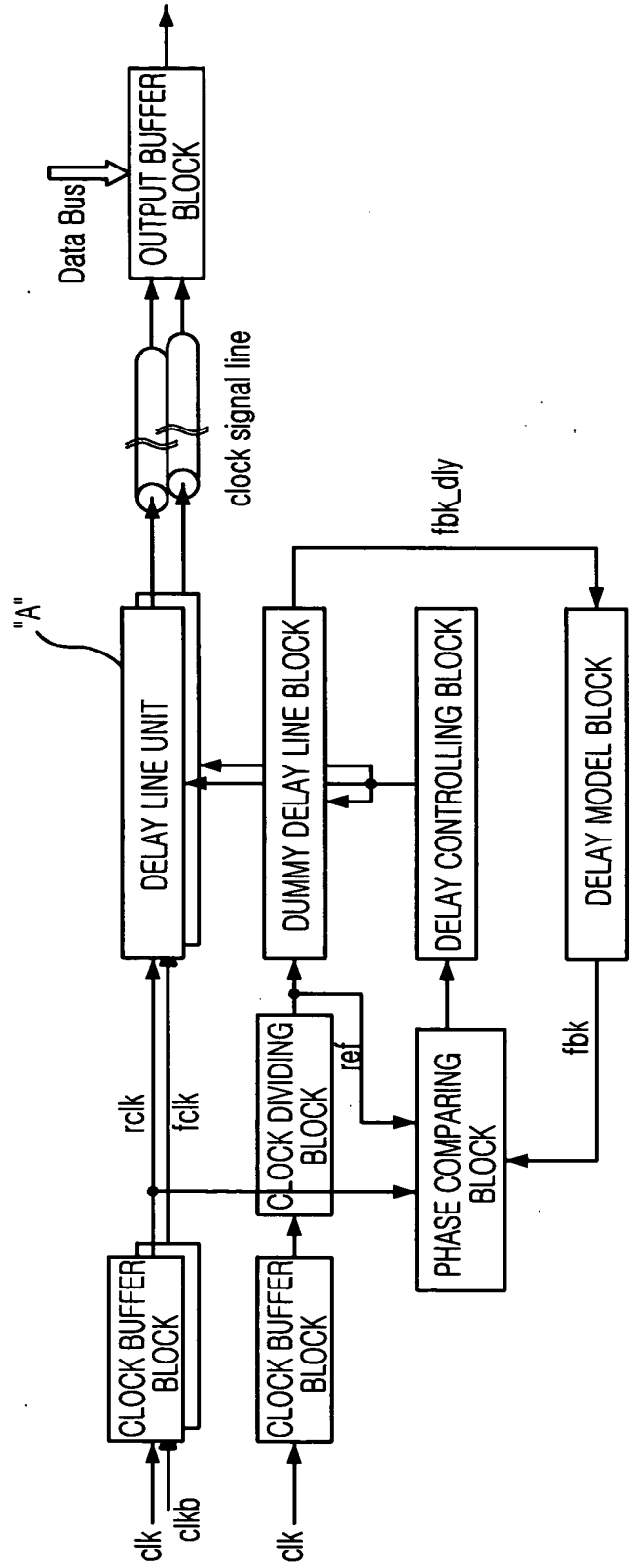
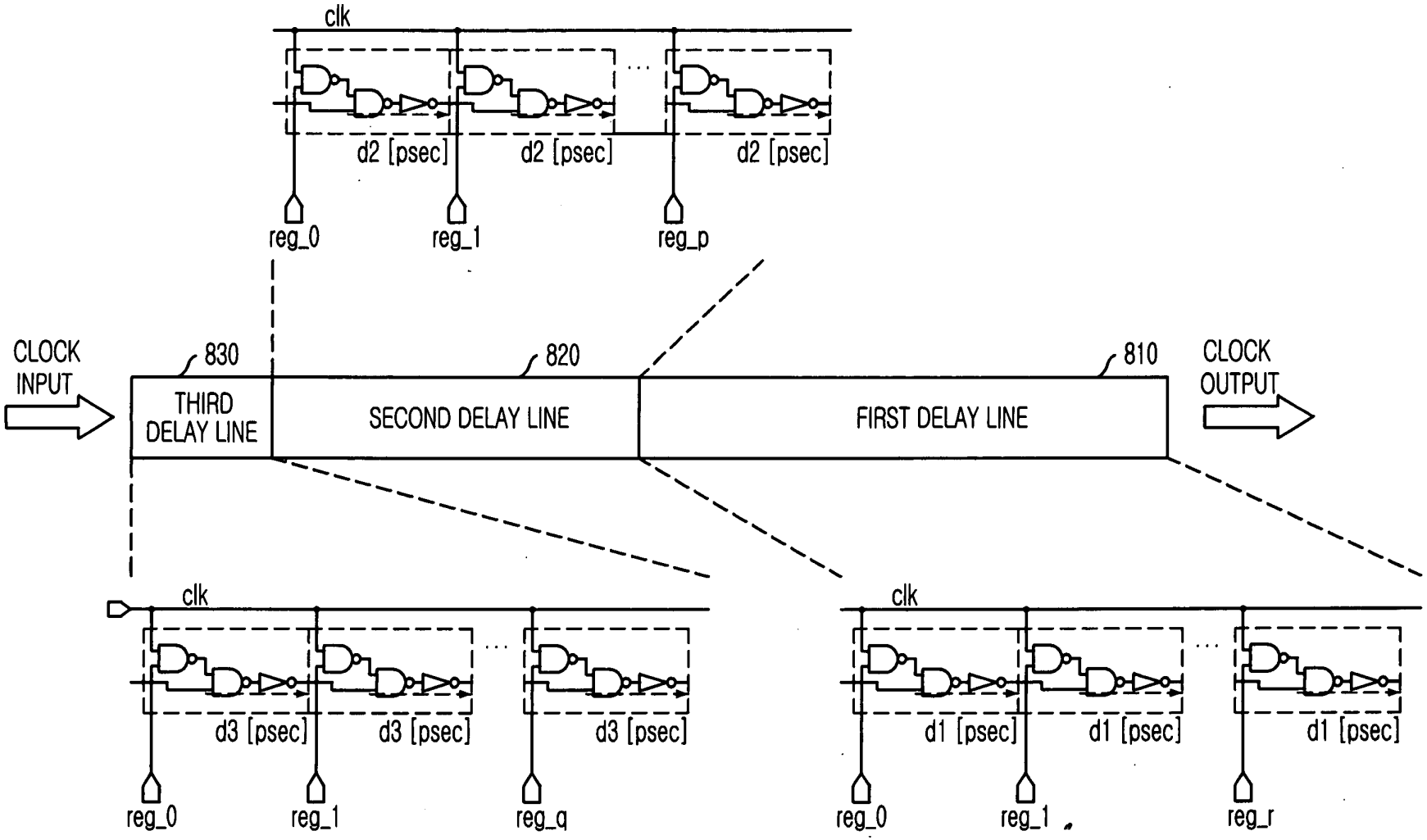

Data Bus
OUTPUT BUFFER BLOCK
clock signal line
"A"
DELAY LINE UNIT
DUMMY DELAY LINE BLOCK
DELAY CONTROLLING BLOCK
DELAY MODEL BLOCK
fbk_dly
rclk
fclk
CLOCK DIVIDING BLOCK
ref
fbk
PHASE COMPARING BLOCK
CLOCK BUFFER BLOCK
CLOCK BUFFER BLOCK
clk
clkb
clk

FIG. 8


clk
d2 [psec]
d2 [psec]
d2 [psec]
reg_0
reg_1
reg_p
CLOCK INPUT
830
820
810
CLOCK OUTPUT
THIRD DELAY LINE
SECOND DELAY LINE
FIRST DELAY LINE
clk
d3 [psec]
d3 [psec]
d3 [psec]
reg_0
reg_1
reg_q
clk
d1 [psec]
d1 [psec]
d1 [psec]
reg_0
reg_1
reg_r